**Amendments to the Specification:**

Please amend the following paragraph beginning at page 3, line 11 as follows:

Japanese Laid Open Patent Application (JP-A-Heisei 10-133958) discloses "COMMUNICATION APPARATUS CONTROL CIRCUIT". This communication apparatus control circuit employs a method of storing a main program for an apparatus control in an electrically erasable writable flash memory. This communication apparatus control circuit comprises a reset counter for detecting that a CPU can not be recovered by a watch dog reset of the CPU and a system error detector. The communication apparatus control circuit further includes an address decoder, which when a system error is detected by the system error detector, compulsorily switches a memory region accessed by the CPU, to a spare memory region in which a down line load function program and a function program to be operated at a time of a spare operation are stored and RAM and ROM for storing the spare program constituting the spare memory region. Due to this configuration, even if the CPU is run away and it can not be recovered by the watch dog reset, the switching to the spare memory region for the processing operation through the spare program enables the down load line ~~load~~ of the main program. Thus it is not necessary to exchange a memory device.

Please amend the following paragraph beginning at page 16, line 24 as follows:

The ASYNC signal lines for the receptions (RDXs of Fig. 1) are connected in parallel. Therefore ~~Therefor~~, the first processor 1 and the second processor 2 receive the same data. Each processor monitors the reception data. If the reception data is the monitor control command, the first processor 1 is operated. In the case of the download command, the second processor 2 is operated. The ASYNC signal lines for the transmission (TXD of Fig. 1) are connected to a gate circuit 4. If only one processor transmits a data, the line TXD is fixed to the HIGH level. The ASYNC signal line for the transmission of the second processor 2 is usually set at the HIGH level since the second processor 2 carries out a communication only when the download command is

transmitted. Thus, the first processor 1 can avoid a signal collision and carry out a communication. When the download command is transmitted, the second processor 2 firstly stores the data in a buffer. Meanwhile, the first processor 1 does not carry out the ASYNC communication, and only the second processor 2 carries out the communication.

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